REMARKS

Claims 21 and 25 are present in this application. Claim 21 has been rejected. Applicants acknowledge, with appreciation, the Examiner's allowance of Claim 25 and supporting reasons therefor.

Rejection Under 35 USC 103(a) of Claim 21 on Huang, et al. in View of Jairazbhoy, et al.

Claim 21 has been rejected under 35 USC 103(a) as unpatentable over U.S. Patent No. 6,521,997 to Huang, et al. in view of U.S. Patent No. 6,303,872 to Jairazbhoy, et al.

It appears to be the Examiner's position in this rejection that Huang, et al. disclose all of the Claim 21 limitations except Huang, et al. fail to teach "that the solder connection is present on the upper contact surface". For the latter, the Examiner relies upon Jairazbhoy, et al. In relying on Jairazbhoy, et al., the Examiner states that Jairazbhoy, et al. disclose that "an optimal solder joint for a two terminal passive device includes solder on the top surface of the lateral contact".

The Examiner goes on to state that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SMD packaging structure of Huang, such that the solder from the lateral solder joint is present on the upper contact surface, as taught by Jairazbhoy". The Examiner goes on to state that "the rationale is as follows: A person having ordinary skill in the art would have been motivated to dispose

solder on the upper contact surface, because Jairazbhoy shows that doing so balances the net forces applied on the SMD during solder reflow, such that the SMD remains properly aligned with the substrate and such that the solder joint has optimal structural integrity".

Applicants acknowledge the Examiner's position outlining the advantages of the Jairazbhoy, et al. solder joint structure but fail to see how the teachings of Jairazbhoy, et al. in relating to this structure could be combined with Huang, et al.

Huang, et al.

The Huang, et al. invention is directed to a chip carrier for accommodating a passive component. The particular chip carrier structure for accommodating a passive component acts to prevent the occurrence of short circuit between the passive component and solder pads.

Specifically, as stated by Huang, et al., the invention proposes "a chip carrier for accommodating a passive component, comprising: a core layer defined with a chip attach area ... and a trace forming area surrounding the chip attach area ...; a solder mask layer applied onto the trace forming area; and at least a pair of spaced-apart solder pads formed on the trace forming area and partly exposed to outside of the solder mask layer, wherein a recessed portion is formed at the solder mask layer between the pair of solder pads" (emphasis added). The above structure allows the passive component and solder connections to be encapsulated, as shown in Figures 3 and 4.

Figure 2 shows solder pads 12 partly exposed to outside the solder mask layer 11. Figure 2 also shows the recessed portion 13 formed at the solder mask layer 11. Figure 3

shows the Figure 2 structure with passive component 15 bonded to solder pads 12 and encapsulated by 17. Figure 4 shows two layers of encapsulant with the inner layer being a resin 18.

Jairazbhoy, et al.

Jairazbhoy, et al. are directed to surface mount devices (SMD) attached to printed circuit board (PCB) substrates. The Jairazbhoy, et al. invention involves specific solder joint structures that act to prevent "tombstoning" as defined in Column 1 of Jairazbhoy, et al. As stated by Jairazbhoy, et al. in Col. 2, lines 8, et seq., "each mounting pad has a predetermined length and each solder joint has a predetermined volume of solder selected such that a positive net anti-tombstoning moment is exerted upon the SMD when at least one solder joint is in a molten state" (emphasis added).

Jairazbhoy, et al. go on to state, starting in Col. 2, lines 65 and into Col. 3, that "in order to optimize the design of the solder joint 50 such that an OTTJ is formed and a positive net anti-tombstoning moment and a positive net recentering force are both exerted on the SMD 30 when the solder 4 point melts, it is necessary to determine the amount of solder to be deposited on each mounting pad in order to form each joint 50, and to specially design the mounting pad length lp such that the forces and moments are arranged as desired while each joint is molten".

Thus, Jairazbhoy, et al. design a solder joint structure that "arranges the pressure forces and surface tension forces in such a way that a positive net anti-tombstoning moment and a positive net recentering force are both exerted on the device 30 by each

solder joint 50 when each solder joint 50 is in a molten state (i.e. after reflow but before cooling of the joint 50)" (Col. 2, lines 59, et seq.) (emphasis added).

The Jairazbhoy, et al. solder joint structure has nothing to do with preventing shorts by encapsulation, as taught by Huang, et al. It is not clear that the Jairazbhoy, et al. specially designed solder joint structure does anything other than prevent tombstoning which, in turn, prevents disconnects from the mounting pads due to decentering. Thus, it is also not clear that the particular solder joint structure of Jairazbhoy, et al. provide "optimal structural integrity", as characterized by the Examiner. The solder joint structure of Jairazbhoy, et al. prevents disconnects "from the mounting pads on the end where the solder paste melted last" (Col. 1, lines 51, et seq.). Jairazbhoy, et al. do not say that their solder joint structure itself provides optimal integrity, i.e., is optimally strong.

Huang, et al., on the other hand, are not addressing the problem of tombstoning or decentering but rather are addressing the problem of short circuiting between pads, which problem they solve by encapsulation. It is not clear to Applicants why one skilled in the art would be motivated to employ the process and structure of Jairazbhoy, et al. for preventing tombstoning in Huang, et al.

Moreover, it is not clear to Applicants how the process and solder joint structure of Jairazbhoy, et al. would be implemented in Huang, et al. It can be seen that the Jairazbhoy, et al. process and structure enabling a positive net anti-tombstoning moment and a positive net recentering force are somewhat detailed and complex. As stated in Col. 4, lines 1, et seq. of Jairazbhoy, et al., "the present invention accomplishes this by providing an appropriate design for the mounting pad length l_p and by determining the volume V needed to be deposited on the mounting pad". Jairazbhoy, et al. go on in their

enabling process description in Col. 2 to refer to dimensions l_i and l_o, the "effective" inner and outer mounting pad extension lengths.

Jairazbhoy, et al. go on further in Col. 4, lines 28, et seq. to describe that one must "determine the dimensions and features for each given SMD 30" which dimensions include "W, d, the number of terminations, H_o (the height of each side termination 44), h (the distance between the top of the mounting pad 20 and the underside of the bottom termination 46 is present) also known as the solder joint height, l_m (the length of the top and optional bottom termination 42/46... w (the width of each termination 40)".

To implement the process of Jairazbhoy, et al. in Huang, et al., it would be necessary to define the corresponding dimension points in Huang, et al. as are defined in Jairazbhoy, et al. However, to do so is quite problematic. For example, is the solder joint height h taken from the top of pad 12 or top of solder mask layer 11?

Additional questions that would arise are, for example;

- Is the mounting pad length l_p to be taken in Huang, et al. the length of pad 12 in total or the length of pad 12 exposed?
- Do the length dimensions l_i and l_o of Jairazbhoy, et al. (I_a and I_l in Figure 3) refer to length taken from the complete length of pad 12 of Huang, et al. or from the exposed length of pad 12?
- How is the volume V of solder to be measured in Huang, et al. i.e., with or without the solder mask 11?
- Does the opening in solder mask 11 exposing a portion of solder pad 12 affect the dynamics of the Jairazbhoy, et al. process and structure? Note that Jairazbhoy, et al. have the complete pad exposed.

- Does the passage 16 affect the dynamics of the Jairazbhoy, et al. process and structure?
- Where is point A in Figure 4 of Jairazbhoy, et al. taken in Huang, et al., at the end of solder pad 12 or at some point on the exposed surface of pad 12?
- How does the solder mask layer 11 of Huang, et al. affect the formation of the convex, continuous substantially circular arc covering substantially ... all of mounting pad 20, as required by Jairazbhoy, et al.? (Col. 4, lines 50 - 56 of Jairazbhoy, et al.).

It is clear from the above examples that the structural differences between Huang, et al. and Jairazbhoy, et al. raise a number of technical questions as to how the Jairazbhoy, et al. process and structure can properly be used in Huang, et al. Stated succinctly, it would seem, at a minimum, that the structural differences involving mask layer 11 of Huang, et al. would prevent using the teachings of Jairazbhoy, et al. in Huang, et al.

Accordingly, Applicants fail to see how one skilled in the art, even if there were a basis for motivation to do so, would be able to employ the teachings of Jairazbhoy, et al. in Huang, et al. Moreover, given the technical issues raised, Applicants believe there would not be a reasonable expectation of success in combining the teachings of Jairazbhoy, et al. in Huang, et al. Thus, Applicants believe that all three criteria required to establish a prima facia case of obviousness fail in this rejection.

Conclusion

In view of Applicants' amendment and remarks, Applicants believe that the claims should now be clearly allowable. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejection, allow Claim 21 as presented, and pass the case to issue.

Respectfully submitted,

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